

Insufficient Solder Volume
SOLVED

SOLDER FORTIFICATION®



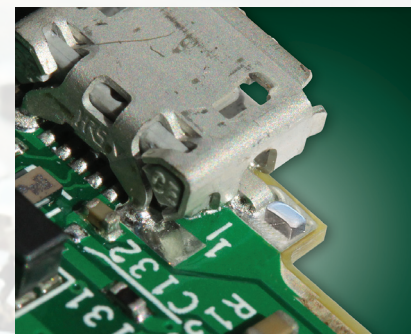
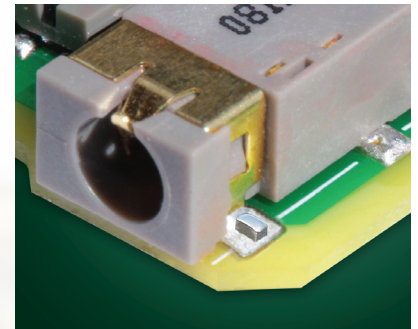
Add Solder Fortification® Preforms to:

Connectors: Improve reliability with added solder
RF Shields: Fortify connections; provide sufficient solder volume

- Thin stencils leave large deposits solder-starved
- Preforms add solder volume without modifying stencil design
- Multiple preforms can be placed in paste to add solder volume exactly where it is needed
- Preforms prevent failures from shock due to insufficient connections

Through-Hole Assemblies: Ensure complete hole fill

- Assemble through-hole parts reliably without wave soldering
- Paste alone will not provide complete hole fill since much of the solder paste volume is approximately 50% flux
- Add a preform to add solder without adding more flux
- Minimize flux pooling around these components
- Preforms allow optimal fillet formation



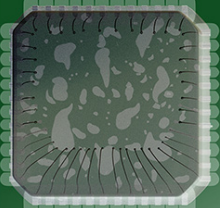
Myth: Only squared preforms can be used for Solder Fortification®

It is not true that only squared or flat-sided preforms can be used for solder fortification. In fact, even spheres have been used to add solder volume.

The key to success for using Solder Fortification® preforms is their ability to be pick and placed easily.

Indium Corporation is the leader in custom designed preforms. Although standard dimensions in tape are 0201, 0603, 0402, and 0805, we also offer custom solutions. Contact us and we will make sure you "pick" the right solution.






QFN Voiding

Solving SMT problems with Solder Preforms

Need a solution to QFN voiding? We wrote the book.
Check our tech papers online or contact us directly
and speak to one of our tech service engineers.



From One Engineer to Another®



Indium Corporation Tech Paper


Minimizing Voiding in QFN Packages Using Solder Preforms

Author: Seth J. Homer and Ronald C. Lasky, PhD, PE.


Abstract
According to Prismark Partners, the use of quad-flat no-leads (QFNs) is growing faster than any package type except for flip-chip CSPs. Prismark projects that by 2013, 32.6 billion QFNs will be assembled worldwide, which represents 15% of all IC packages.

However, QFNs can be a challenge to assemble, especially when it comes to voiding. In most QFN assembly processes, solder paste is used as a means of attachment. This approach can be problematic, as excessive voiding often occurs due to the lack of standoff on the component and the high flux content of the

SETH HOMER



Seth Homer, Product Support Specialist




Indium Corporation Tech Paper

The Effect of Thermal Pad Patterning on QFN Voiding


Author: Derrick Herron, Dr. Yan Liu, and Dr. Ning-Cheng Lee.

Abstract
Voiding under QFNs is a major challenge in the electronics industry. However, voiding can be suppressed by improving venting accessibility on the thermal pad by using solder mask dividing strips. Venting accessibility is defined as the perimeter length per unit area of the metal pad. Regardless of the shape and the number of subpads, increasing venting accessibility results in a decrease in the total number of voids, the largest voids, and discontinuity. Voiding caused by peripheral vias is comparable to voids caused by hidden vias. Voiding increases with decreasing print coverage and is attributed to insufficient solder. Voiding also decreases with an increase in the number of thermal vias. This phenomenon is attributed to volatiles bleeding through the small voids around the thermal via

DR. NING-CHENG LEE



Dr. Ning-Cheng Lee, Vice President of




Indium Corporation Tech Paper

Influence of Reflow Profile and Pb-Free Solder Paste in Minimizing Voids for Quad Flat Pack No-Lead (QFN) Assembly

Author: Harish Gadepalli, Rangaraj Dhanasekaran, Dr. S. Manian Ramkumar, Tim Jensen, and Ed Briggs

Abstract
Quad Flat Pack No-lead (QFN) packages have become a popular choice in electronics packaging due to their small form factor. They are also gaining rapid industry acceptance because of its excellent thermal and electrical performance. The bottom side of the QFN package has a large thermal pad. This exposed die attach pad effectively conducts heat to the PCB and also provides a stable ground connection. Effective soldering of this surface to the pad on the PCB is required for good thermal dissipation and component functionality. The exposed thermal pad presents various challenges during the surface mount assembly process. One major challenge is solder void

TIM JENSEN




Indium Corporation Tech Paper

Thermal Pad Design and Process for Voiding Control at QFN Assembly

Author: Derrick Herron, Dr. Yan Liu, and Dr. Ning-Cheng Lee.

Abstract
Quad-flat no-leads (QFN) package designs are receiving more and more attention in the electronics industry. This package offers a number of benefits including (1) small size, such as a near die size footprint, thin profile, and light weight; (2) easy PCB trace routing due to the use of perimeter I/O pads; (3) reduced lead inductance; and (4) good thermal and electrical performance due to the adoption of exposed copper die-pad technology. These features make the QFN an ideal choice for many new applications where size, weight, electrical, and thermal properties are important. However, the adoption of QFN often runs into voiding issue at SMT assembly. Upon reflow, outgassing of solder paste flux at the large thermal pad has difficulty escaping

DR. NING-CHENG LEE



Dr. Ning-Cheng Lee, Vice President



Indium Corporation Tech Paper

How to Reduce Voiding in Components with Large Pads

Author: Wisdom Qu.

Introduction
As the electronics industry moves toward miniaturization and multifunction, smaller components with more functions, such as quad-flat no-leads (QFNs) and LGAs, are increasingly used in a variety of products.

QFNs, being a near chip-scale package, have perimeter contacts on the package bottom providing electrical connections

outgassing from solder paste on the thermal pad with vias forms bubbles. With the SMT process, difficulty in venting the outgas causes large voids to form. We can only try to find solutions to minimize voiding although it is almost impossible to prevent it from happening.

The land grid array (LGA) package looks very similar to a BGA package. It has flat contacts arranged in array on the bottom

WISDOM QU




Indium Corporation Tech Paper

Voiding Control for QFN Assembly

Author: Derrick Herron, Dr. Yan Liu, and Dr. Ning-Cheng Lee

Abstract
Quad Flat No Leads (QFN) package designs receive more and more attention in electronic industry nowadays. This package offers a number of benefits including (1) small size, such as a near die-sized footprint, thin profile, and light weight; (2) easy PCB trace routing due to the use of perimeter I/O pads; (3) reduced lead inductance; (4) easy PCB trace routing; and (5) good thermal and electrical performance due to the adoption of exposed copper die-pad technology. These features make the QFN an ideal choice for many new applications where size, weight, electrical, and thermal properties are important. However, adoption of QFN often runs into voiding issues at SMT assembly. Upon reflow, outgassing

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