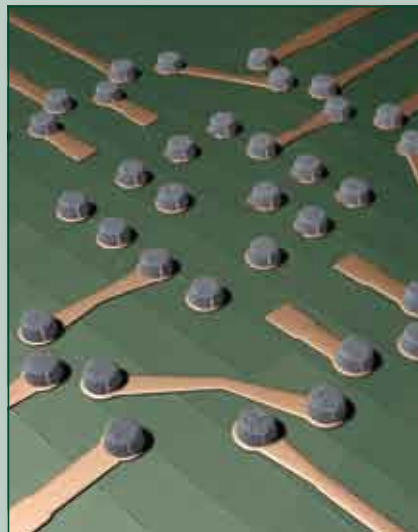


Indium8.9

Pb-Free No-Clean Solder Paste

- Low voiding at via-in-pad
- Unsurpassed response-to-pause printing
- Excellent wetting
- Clear, probe testable flux residue



Product Information

Indium8.9 Pb-Free No-Clean Solder Paste

Features

- High transfer efficiency through small apertures ($\leq 0.66AR$)
- Excellent wetting to all common finishes at high and low peak reflow temperatures
- Clear, probe testable flux residue
- Eliminates head-in-pillow defects

Introduction

Indium8.9 is an air reflow, no-clean solder paste specifically formulated to accommodate the higher processing temperatures required by the Sn/Ag/Cu, Sn/Ag, and other alloy systems favored by the electronics industry to replace conventional Pb-bearing solders. **Indium8.9** offers unprecedented stencil print transfer efficiency to work in the broadest range of processes. In addition, the high probe testability of **Indium8.9** minimizes false failures in ICT.

Alloys

Indium Corporation manufactures low-oxide spherical powder composed of a variety of Pb-Free alloys that cover a broad range of melting temperatures. Type 4 and Type 3 powder are standard offerings with SAC305 & SAC387 alloys. The metal percent is the weight percent of the solder powder in the solder paste and is dependent upon the powder type and application. Standard product offerings are detailed in the above right table.

Standard Product Specifications

Alloy	Metal Load	IPN
96.5Sn/3.0Ag/0.5Cu (SAC305)	88.25% (Type 4)	800420
96.5Sn/3.0Ag/0.5Cu (SAC305)	88.50% (Type 3)	800449

Packaging

Indium8.9 is currently available in 500g jars or 600g cartridges. Packaging for enclosed print head systems is also readily available. Alternate packaging options may be available upon request.

Storage and Handling Procedures

Refrigerated storage will prolong the shelf life of solder paste. The shelf life of **Indium8.9** is 6 months when stored at $<10^{\circ}C$. Solder paste packaged in cartridges should be stored tip down.

Solder paste should be allowed to reach ambient working temperature prior to use. Generally, paste should be removed from refrigeration at least two hours before use. Actual time to reach thermal equilibrium will vary with container size. Paste temperature should be verified before use. Jars and cartridges should be labeled with date and time of opening.

Material Safety Data Sheets

The MSDS for this product can be found online at <http://www.indium.com/techlibrary/msds.php>.

Bellcore and J-STD Tests & Results

J-STD-004A (IPC-TM-650)	Result	J-STD-005 (IPC-TM-650)	Result
Flux Type (per J-STD-004A)*	ROL1	Typical Solder Paste Viscosity: Malcom (10rpm)	
Flux Induced Corrosion: Copper Mirror	Type L	Type 4	2050 poise
		Type 3	2200 poise
Presence of Halide		Slump Test	Pass
Silver Chromate	Pass	Solder Ball Test	Pass
Fluoride Spot Test	Pass	Typical Tackiness	50g
Ion Chromatography	$<0.5\% Cl^{-}$ eq.	Wetting Test	Pass
Post Reflow Flux Residue: ICA Test	35%		
SIR	Pass	Bellcore GR-78	Result
* J-STD-004A has replaced J-STD-004 and is more stringent in its requirements.		SIR	Pass
		Electromigration	Pass

All information is for reference only. Not to be used as incoming product specifications.

Indium8.9 Pb-Free No-Clean Solder Paste

Printing

Stencil Design:

Electroformed and laser cut/electropolished stencils produce the best printing characteristics among stencil types. Stencil aperture design is a crucial step in optimizing the print process. The following are a few general recommendations:

- Discrete components — A 10-20% reduction of stencil aperture has significantly reduced or eliminated the occurrence of mid-chip solder beads. The “home plate” design is a common method for achieving this reduction.
- Fine pitch components — A surface area reduction is recommended for apertures of 20 mil pitch and finer. This reduction will help minimize solder balling and bridging that can lead to electrical shorts. The amount of reduction necessary is process dependent (5-15% is common).
- For optimum transfer efficiency and release of the solder paste from the stencil apertures, industry standard area ratios should be adhered to.

Printer Operation:

The following are general recommendations for stencil printer optimization. Adjustments may be necessary based on specific process requirement:

- Solder Paste Bead Size: 20-25mm diameter
- Print Speed: 50-100mm/sec
- Squeegee Pressure: 0.018-0.027kg/mm of blade length
- Underside Stencil Wipe: Start at once every 5 prints then decrease frequency until an optimum value is determined.
- Solder Paste Stencil Life: >8 hrs. @ 30-60% RH & 22°-28°C

Cleaning

Indium8.9 is designed for no-clean applications; however, the flux can be removed if necessary by using a commercially available flux residue remover.

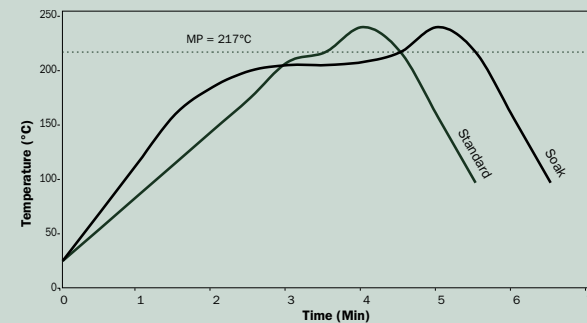
Stencil Cleaning is best performed using isopropyl alcohol (IPA) as a solvent. Most commercially available stencil cleaners work well.

Compatible Products

- Rework Flux: **TACFlux® 020B**
- Cored Wire: **CW-501, CW-801**
- Wave Flux: **WF-7742, WF-9942**

Reflow

Recommended Profile:



The stated profile recommendations apply to most Pb-Free alloys in the Sn/Ag/Cu (SAC) alloy system, including SAC 305 (96.5Sn/3.0Ag/0.5Cu). This can be used as a general guideline in establishing a reflow profile when using **Indium8.9** Solder Paste. Deviations from these recommendations are acceptable, and may be necessary, based on specific process requirements, including board size, thickness & density.

Heating Stage:

A linear ramp rate of 0.5°- 2.0°C/second allows gradual evaporation of volatile flux constituents and helps minimize defects such as solder balling and/or beading and bridging resulting from hot slump. It also prevents unnecessary depletion of fluxing capacity when a high peak temperature and extended time above liquidus is used. A profile with a soak between 200°-210°C for up to 2 minutes can be implemented to reduce void formation on BGA & CSP type devices. A short soak of 20-30 seconds just below the melting point of the solder can help minimize tombstoning.

Liquidus Stage:

A peak temperature of 12° to 43°C above the melting point of the solder alloy is recommended to achieve acceptable wetting and form a quality solder joint. The time above liquidus (TAL) should be 30–90 seconds. A peak temperature and TAL above these recommendations can result in excessive intermetallic formation that can decrease solder joint reliability.

Cooling Stage:

A rapid cool down of greater than 2°C/second is desired to form a fine grain structure which helps solder joint fatigue resistance.

This product data sheet is provided for general information only. It is not intended, and shall not be construed, to warrant or guarantee the performance of the products

described which are sold subject exclusively to written warranties and limitations thereon included in product packaging and invoices.

Head-in-Pillow Defect: Solved

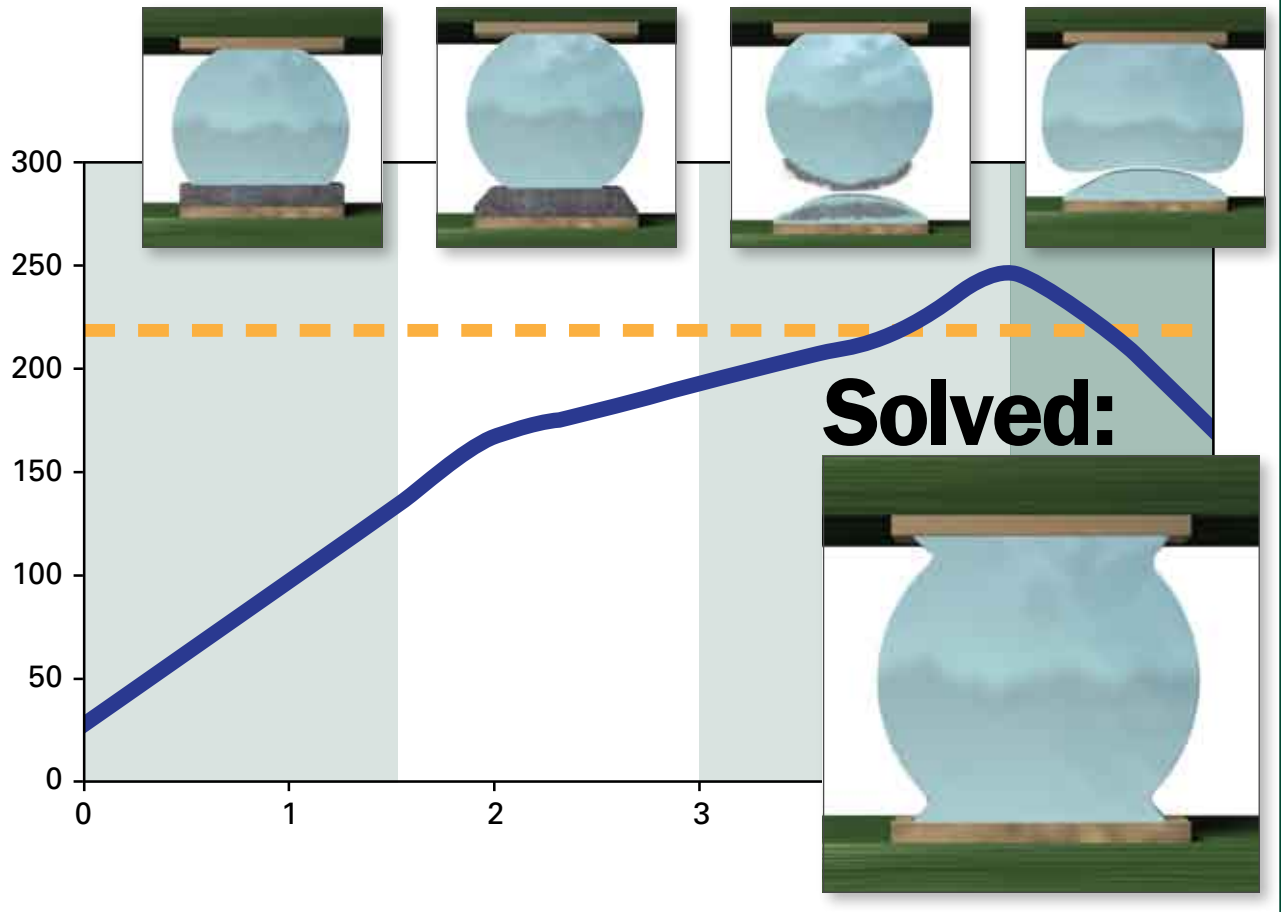
Head-in-Pillow Definition:

A defect in which both the solder paste and the BGA ball reflow but they do not coalesce together.

Causes:

- Component Warping
- Paste Slump
- Poor Wetting
- Alloy Differences

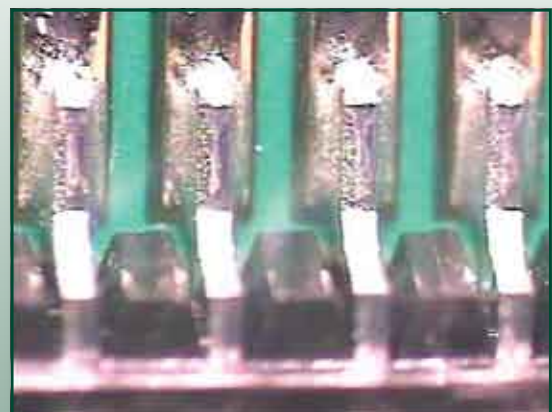
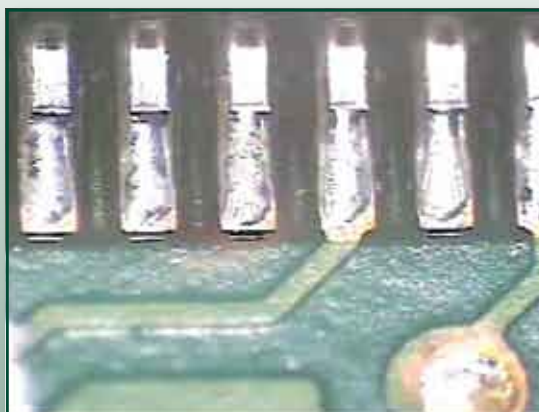
Problem:



Indium8.9 Solutions to Head-in-Pillow Defect

Excellent Wetting

Excellent wetting allows ball and paste to coalesce together at reflow.



Indium8.9 Solutions to Head-in-Pillow Defect

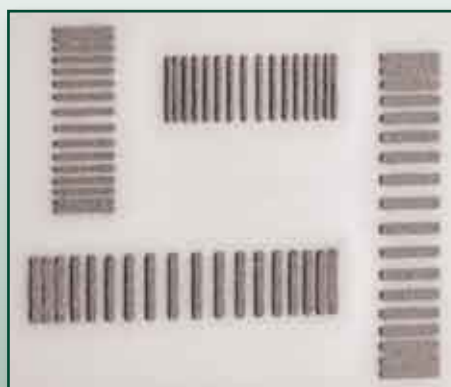
Slump Resistance

No slumping which allows paste to stay in contact with solder ball.



Before

[IPC-A-21 (0.2 mm thickness)]



After

5 min@ 150°C

[IPC-A-21 (0.2 mm thickness)]

High Tack

Paste to remain in contact with ball even if the component warps.

20% RH

Time	Tack	% Change	Post-work	% Change
Initial	48	XXXXXX	37	XXXXXX
1 hour	51	6%	37	0%
4 hour	51	6%	36	-3%
6 Hour	53	10%	38	3%
8 Hour	54	13%	41	11%

47% RH

Time	Tack	% Change	Post-work	% Change
Initial	48	XXXXXX	37	XXXXXX
1 hour	51	6%	33	-11%
4 hour	50	4%	38	3%
6 Hour	50	4%	38	3%
8 Hour	51	6%	38	3%

76% RH

Time	Tack	% Change	Post-work	% Change
Initial	48	XXXXXX	37	XXXXXX
1 hour	49	2%	37	0%
4 hour	49	2%	34	-8%
6 Hour	53	10%	41	11%
8 Hour	51	6%	38	3%

In-Circuit Probe Testing

Board Preparation:

- Print Topside
 - 0.010" Stencil Thickness
 - 0.050" to 0.070" Apertures
- Paste is forced into vias
- Reflow
- Wait 24 hours

Probe Set-Up:

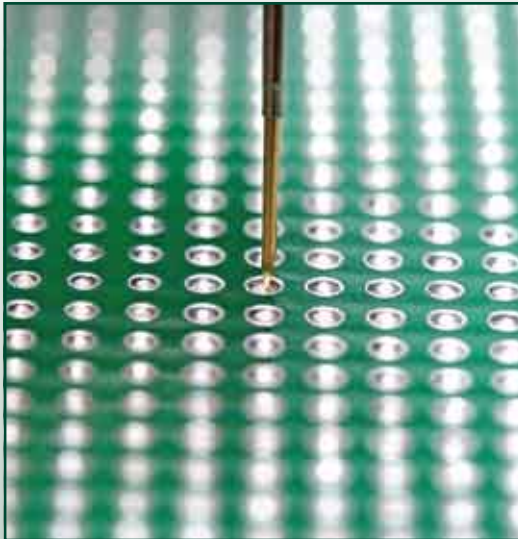
- Verify probe force generated at 2/3 travel
- Connect the test probe onto the auto-dispense head
- Set the required probe travel

Conduct Test:

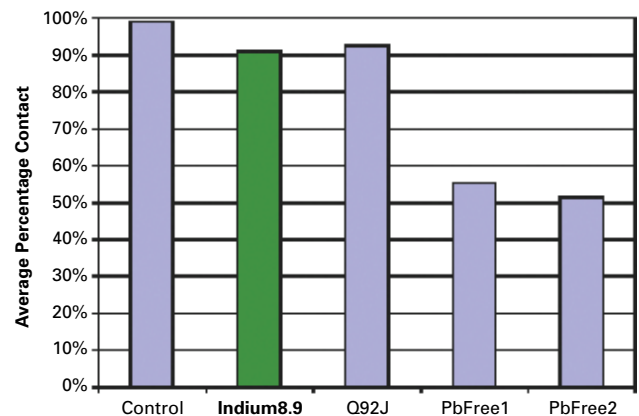
- Probe Test Top & Bottom of Board
- 3 Boards Per Test
 - 5400 test points

Test Vehicle & Probe:

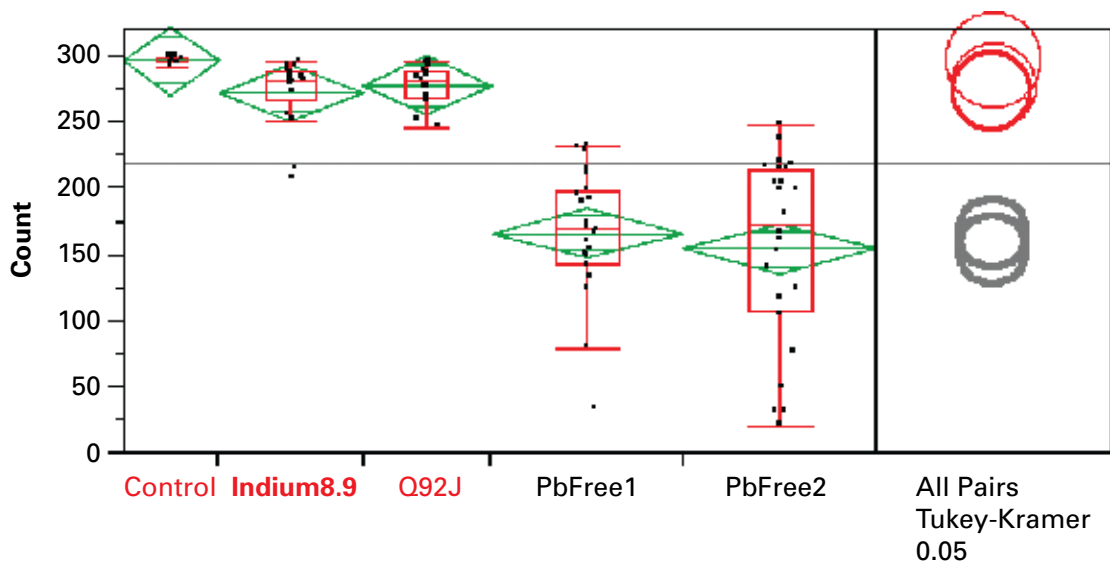
- OSP Board, Double Sided
- 900 Plated Through Hole Vias Per Side
 - 300 Vias per each diameter
 - Diameter Sizes
- Zone 1 0.030"
- Zone 2 0.040"
- Zone 3 0.050"
- 10 Degree Chisel Probe
 - QA part #100-PRP2553X-S
 - Force varies with via size & hole fill (300gms)



Summary Results



Statistical Analysis

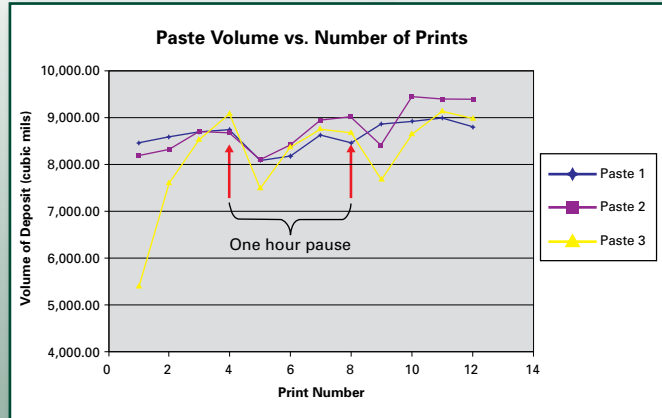
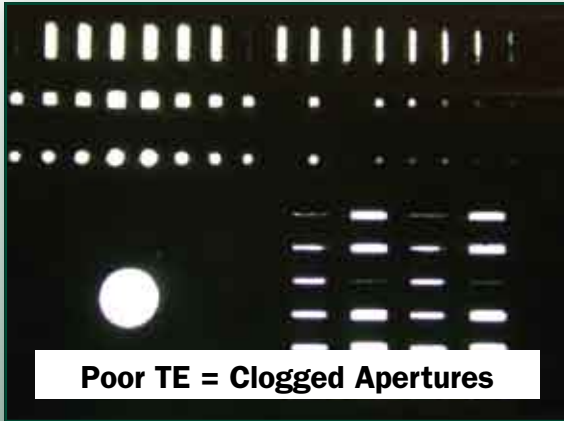


Ultra-Fine Pitch Printing

The stencil printing process is an integral part of achieving high yields in the SMT process. The volume of solder paste stencil printed onto a PCB is critical for minimizing soldering related defects.

$$\text{Transfer Efficiency} = \frac{\text{Actual Stencil Printed Paste Volume}}{\text{Theoretical Maximum Paste Volume}}$$

Response-to-Pause: The ability of a solder paste to print at a high transfer efficiency on the first print after an extended downtime.



Transfer Efficiency (volume%):

Indium8.9

Area Ratio for 5 mil Stencil Apertures

Aperture Shapes

C20

C18

C16

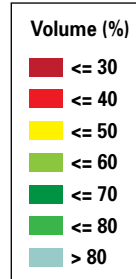
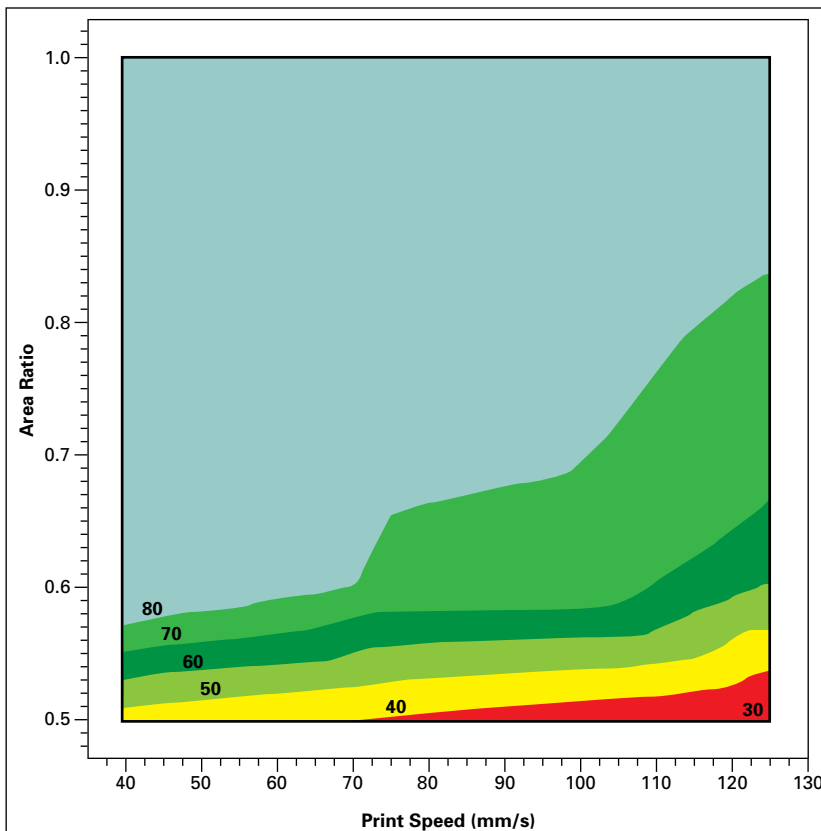
C14

C12

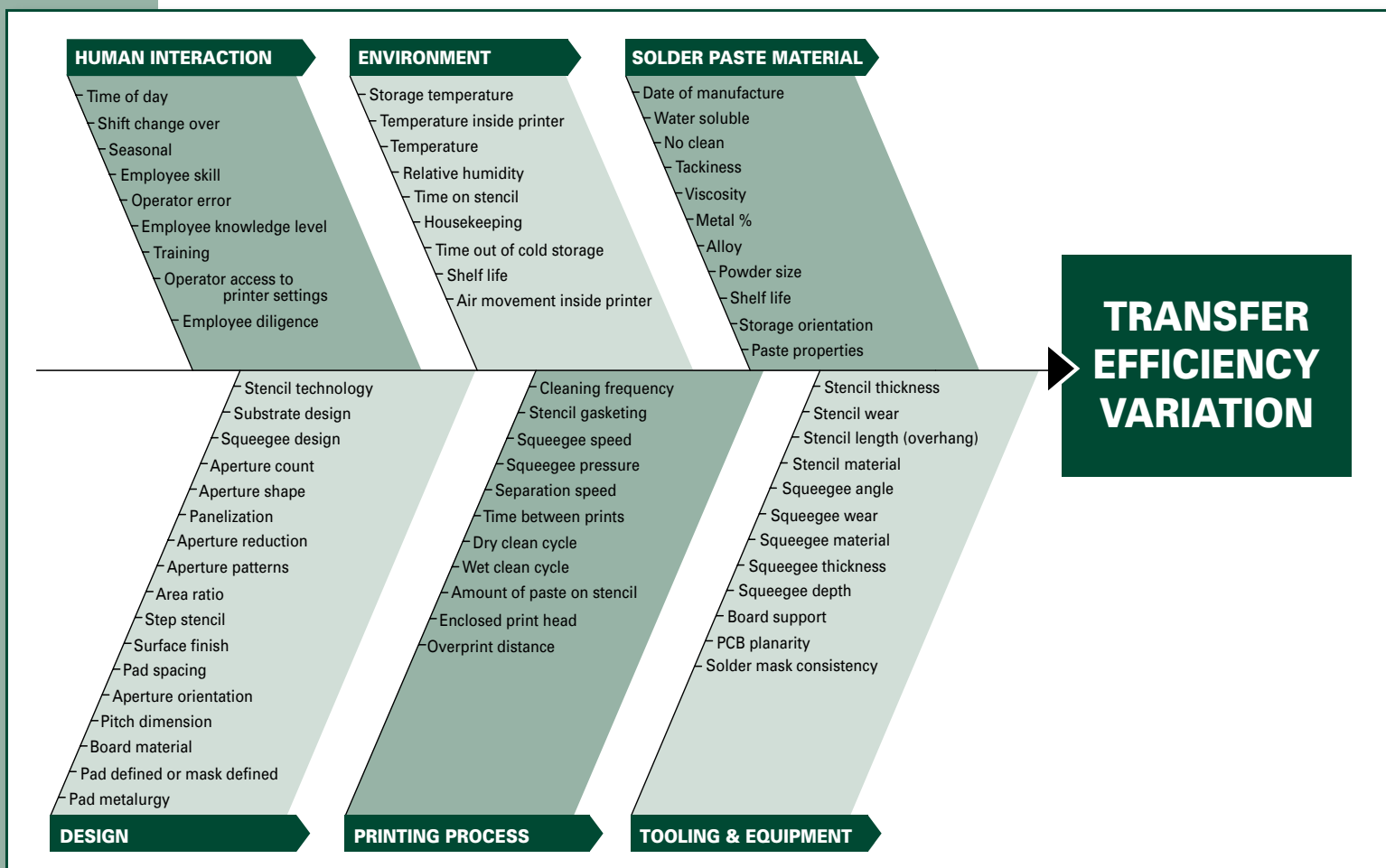
CSP

C10

Contour Plot for Volume (%)



Ultra-Fine Pitch Printing (CONTINUED)



Solder Powder Reference

Solder Powder Size		Stencil Printing				Dispensing			
J-STD-005 Designation	Diameter Range (microns)		Aperture Width		Particles to Span Width		Needle Size		# of Large Particles
			Microns	Inches	Smallest	Largest	Gauge	ID (microns)	
3	25	45	250	0.010	10.00	5.60	22	410	9.1
4	20	38	225	0.009	11.25	6.00	23	330	8.6
5	15	25	200	0.008	13.30	8.00	25	250	10.0
6	5	15	175	0.007	35.00	11.67	27	200	13.3

To ensure that a consistent volume of solder paste is printed onto the board, it is essential to design the stencil according to industry guidelines:

Area Ratio ≥ 0.66

Minimum number of solder particles spanning an aperture should be at least 4-5

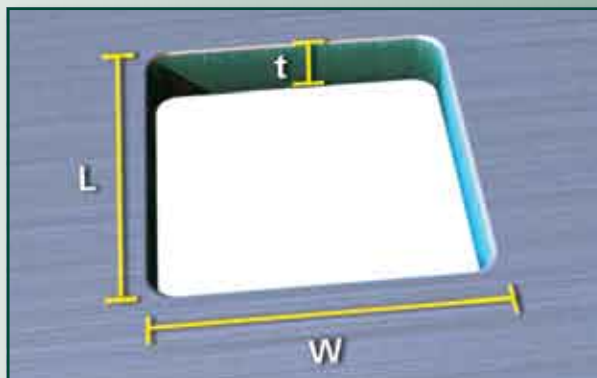
Area Ratio For Square/ Rectangular Apertures

$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$

$$\text{Area Opening} = L \times W$$

$$\text{Area Walls} = 2t(L + W)$$

$$\text{Area Ratio} = \frac{L \times W}{2t(L + W)}$$



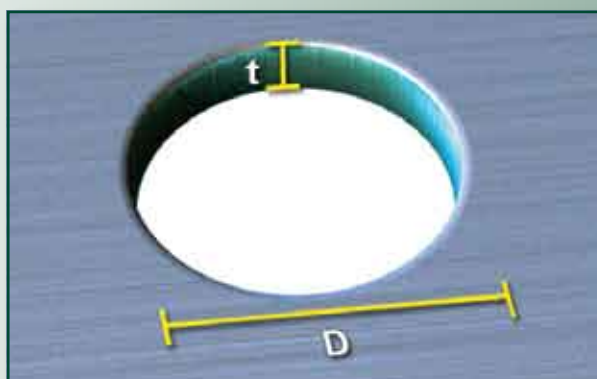
Area Ratio For Circular Apertures

$$\text{Area Ratio} = \frac{\text{Area Opening}}{\text{Area Walls}}$$

$$\text{Area Opening} = \frac{\pi D^2}{4}$$

$$\text{Area Walls} = \pi D t$$

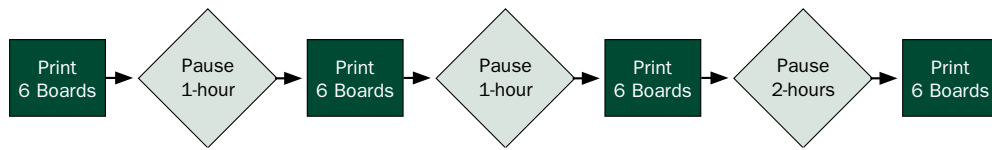
$$\text{Area Ratio} = \frac{D}{4t}$$



Sample Area Ratio Chart

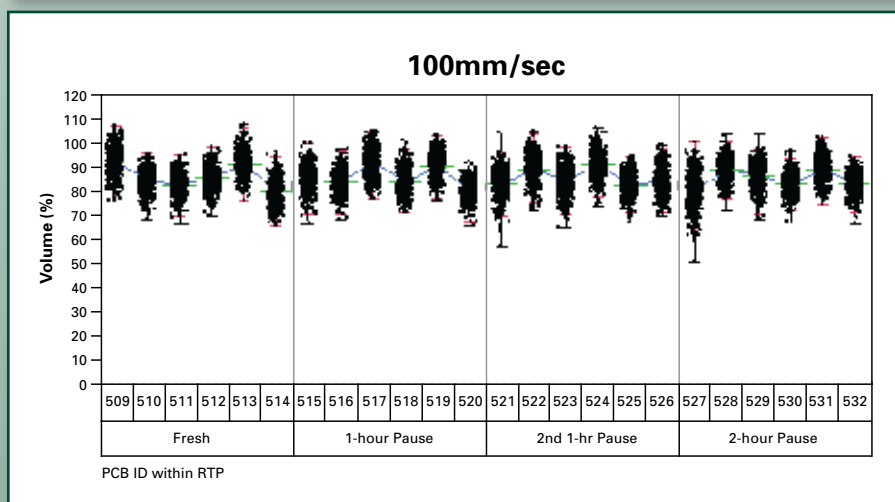
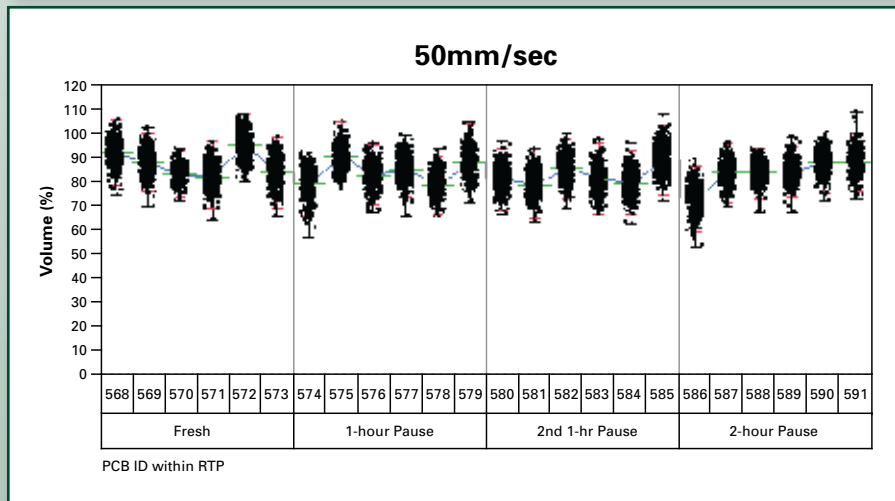
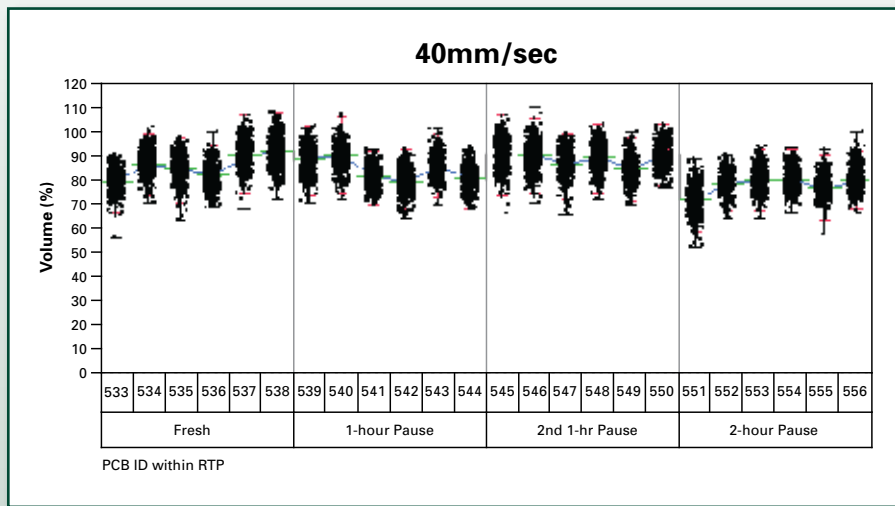
Pad Size (mm)	0.05	0.10	0.15	01005	0.20	0.25	0201	0.30	0.35	0.40	0.45	0.50
Aperture Width (mil)	2.0	3.9	5.9	7 x 8	7.9	9.8	10 x 12	11.8	13.8	15.7	17.7	19.7
Stencil Thickness (5.0 mil)	0.10	0.20	0.30	0.37	0.39	0.49	0.55	0.59	0.69	0.79	0.89	0.98
Stencil Thickness (4.5 mil)	0.11	0.22	0.33	0.41	0.44	0.55	0.61	0.66	0.77	0.87	0.98	1.09
Stencil Thickness (4.0 mil)	0.12	0.25	0.37	0.47	0.49	0.62	0.68	0.74	0.86	0.98	1.11	1.23
Stencil Thickness (3.5 mil)	0.14	0.28	0.42	0.53	0.56	0.70	0.78	0.84	0.98	1.12	1.27	1.41
Stencil Thickness (3.0 mil)	0.16	0.33	0.49	0.62	0.66	0.82	0.91	0.98	1.15	1.31	1.48	1.64
Stencil Thickness (2.5 mil)	0.20	0.39	0.59	0.75	0.79	0.98	1.09	1.18	1.38	1.57	1.77	1.97

Response-to-Pause Procedure



Indium8.9

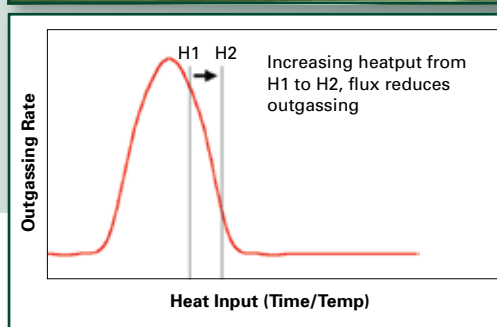
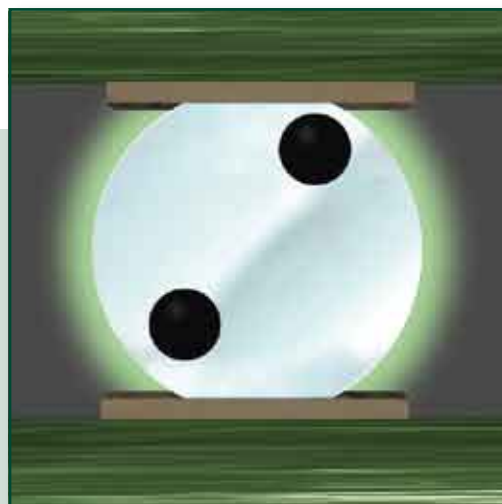
12-mil Round Apertures 5-mil Laser cut Electropolished stencil



Void Characterization

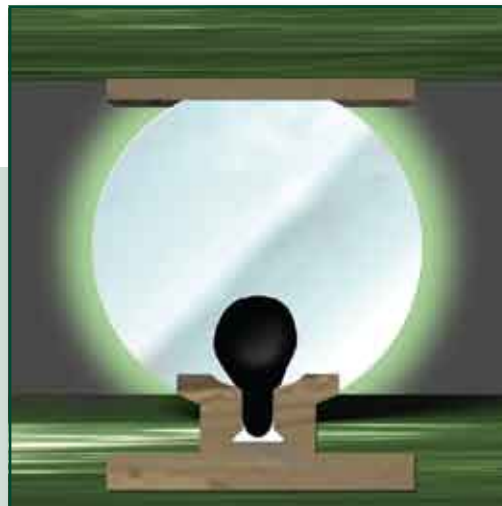
Flux-Induced Voiding

Large voids within solder joints are typically associated with the flux chemistry component of the solder paste. When the solder becomes molten, any entrapped flux that vaporizes has the potential to create a large void. Flux induced voids can be minimized by using a soak profile. This adds additional dwell time to allow the flux to volatilize before the solder reaches its melting point. Peak temperature should also be as low as possible for the given process. Since outgassing is a function of time and temperature, a low peak temperature will minimize flux outgassing.



Microvia-in-Pad Voiding

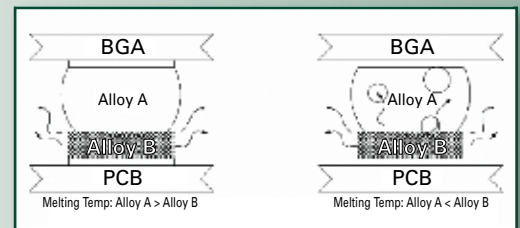
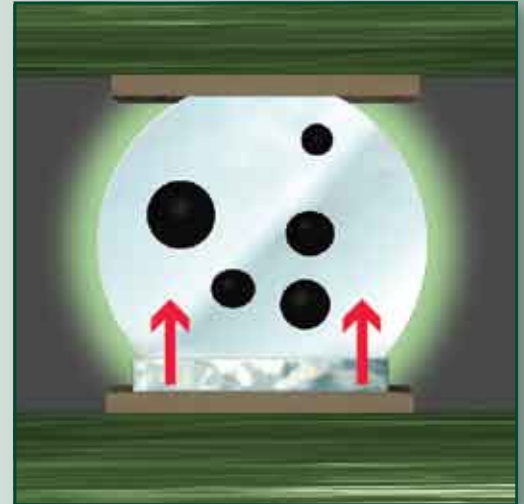
Minimizing microvia-in-pad voiding is challenging because the solder paste needs to be deposited into extremely small via holes. This can cause flux entrapment, which then leads to voiding. When the entrapped flux volatilizes, it has no where to go, thus forming voids similar to those identified in “flux induced voiding” above. Several other factors can contribute to microvia-in-pad voiding, such as poor wetting into the via sub-optimal plating quality, as well as the type of solderability protectant (OSP, ImAg, etc.). In addition, the approaches identified in “flux induced voiding” for void minimization can be used to control microvia-in-pad voids.



Void Characterization (CONTINUED)

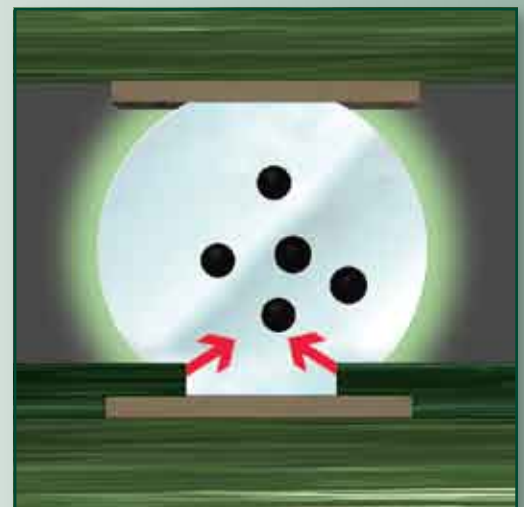
Mixed Alloy Voiding

This condition occurs because the solder paste alloy is different than the alloy used for the BGA ball. The alloy mismatch can generate voids due to the difference in melting temperatures and the subsequent outgassing associated with alloy melting sequence. In the first scenario, the solder paste has a higher melting point than the BGA ball (i.e. SAC paste and Sn/Pb ball). This means that the ball melts first, allowing the molten solder to envelop the solid solder paste. Hence, the flux in the solder paste then outgases directly into the molten solder, which can generate significant voids in the newly formed solder joint. The second scenario is where the BGA ball has a higher melting point than the solder paste (i.e. SAC Ball and Sn/Pb solder paste). This causes the solder paste to melt first, allowing the molten solder to envelop the solid BGA ball. In this situation, a reflow profile can be chosen that allows both alloys to become completely molten and mix together into a uniform solder joint. However, this often requires using a peak temperature higher than that recommended for the solder paste. High peak temperatures can generate additional outgassing of the flux remnant from the solder paste. The best approach for minimizing mixed alloy voiding is to avoid dissimilar alloy designs and only build assemblies with the same alloy.



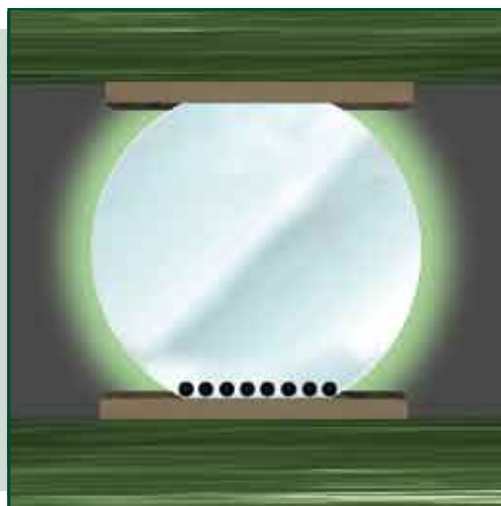
Moisture Related Voiding

Moisture outgassing from the printed circuit board, or from the BGA component itself, is also a potential source of voiding. This is particularly true for solder mask defined pads in which the PCB was left in a condition that promoted moisture absorption. During reflow, the moisture from the solder mask can outgas directly into the molten solder, causing significant voiding. Pre-baking the boards and/or components prior to assembly can be used to verify whether moisture is the source of the voiding. In addition, a long soak profile may help this condition by drying the boards prior to the solder going molten.



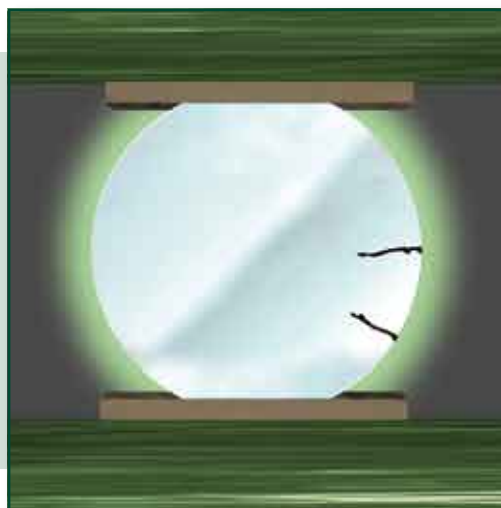
Champagne Voiding

Champagne voids are very small voids (typically 25 microns or smaller) that only appear at the board-to-solder interface. This type of voiding is most commonly reported on Immersion Ag surface finishes. The primary mechanism for champagne voiding is related to the Cu microetch and the Ag immersion plating process used by the board fabricator. There does not appear to be anything within the SMT process set-up that will significantly improve champagne voiding.



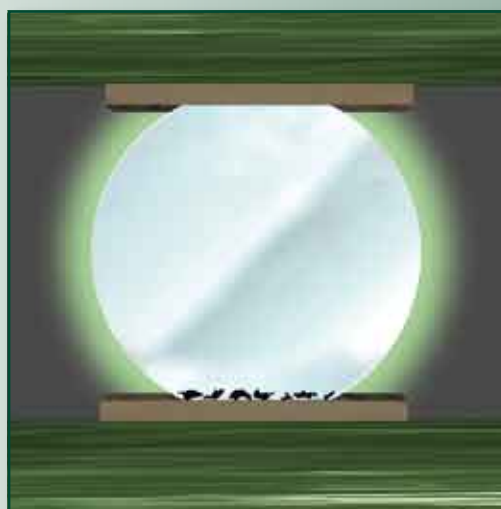
Shrinkage Voiding

Shrinkage voids are vacancies within the solder joint that appear on the surface of the solder joint. These occur during the solidification process of predominantly SAC solders. Shrinkage voids appear to be more prevalent when the cooling rate is slow from peak temperature to the end of the profile. There is no indication that shrinkage voids impact the solder joint reliability.



Kirkendall Voiding

Kirkendall voiding is a phenomenon related to the intermetallic formation of a Cu/Sn alloy matrix. When the solder joint solidifies, the intermetallic becomes the bond mechanism between the bulk solder and the Cu pad on the circuit board. Over time, and particularly at elevated temperatures, the Cu/Sn intermetallic will increase in thickness. This intermetallic growth is caused by the solid state diffusion of the Cu and Sn into one another. The Cu diffuses into Sn much faster than Sn diffuses into Cu, which results in vacancies forming throughout the intermetallic bond area. Changing the reflow profile does not appear to have an impact on Kirkendall voiding, but soldering to Ni surfaces, such as ENIG, can eliminate the potential for Kirkendall voids.



Optimizing Reflow

Section #1 – Preheat:

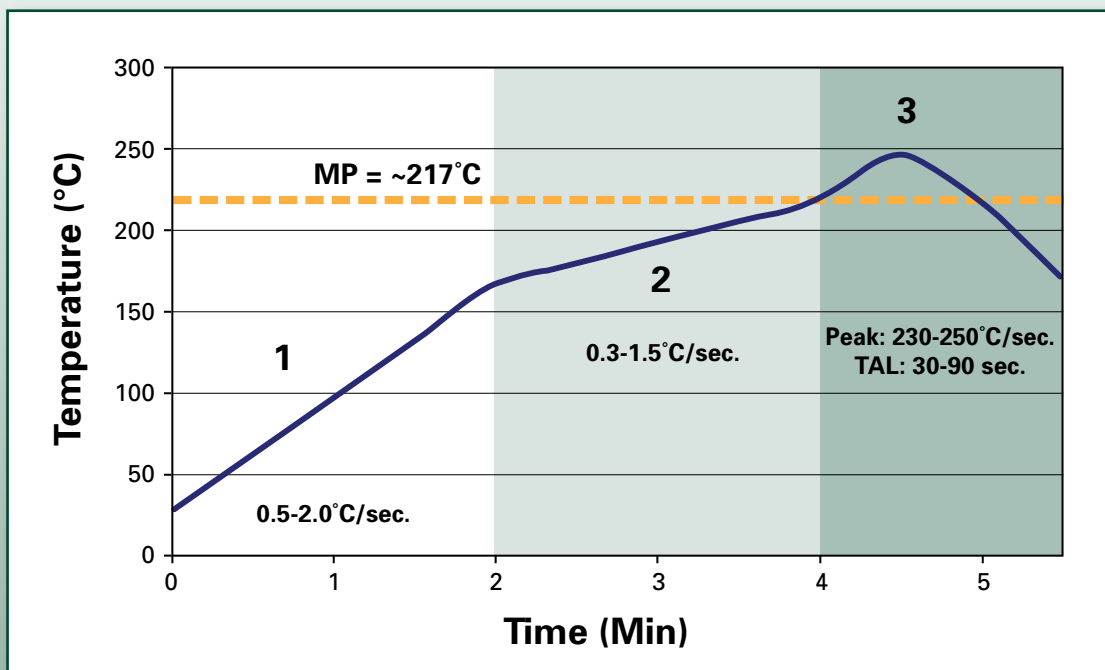
- **Slow Ramp Rate** – Minimizes paste slump and flux spattering. Fewer shorts, solder balls, and solder beads.
- **Fast Ramp Rate** – Minimizes additional oxidation on parts and boards. May help soldering of highly oxidized components.

Section #2 – Soak:

- **Short Soak Time** – Minimizes oxidation and provides best opportunity for good wetting and shiny solder joints.
- **Long Soak Time** – Minimizes tombstoning and voiding. Could negatively impact wetting.

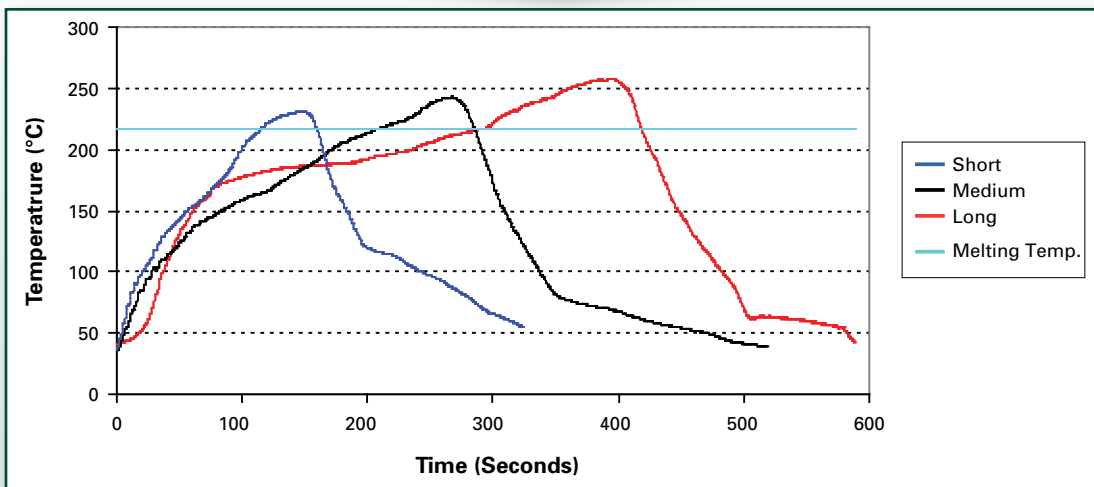
Section #3 – Time Above Liquidus (TAL)/Peak:

- **Short TAL/Low Peak** – Minimizes voiding and thermal damage to components/substrates.
- **Long TAL/High Peak** – Improves solder coalescence but could result in dewetting if too long/high.



Wide Reflow Process Window

Indium8.9



Profile Images

Type	Short Profile	Medium Profile	Long Profile
Solder Balling			
Wetting on ENIG			
Wetting on OSP			
Wetting on ImAg			
Wetting on ImSn			

IPC/J-STD-004A Product Level Testing

Copper Mirror (Test #2.3.32)

Objective: The purpose of this test is to determine the corrosive (free-halide) properties of a flux.

Procedure: Flux is applied to a copper-coated glass slide and sits in a controlled environment for 24 hours. The flux is cleaned and the copper inspected for corrosion.

Results and Image: Pass



Silver Chromate (Test #2.3.33)

Objective: The purpose of this test is to determine the corrosive (free-halide) properties of a flux.

Procedure: Flux is applied to Silver Chromate-impregnated paper, and inspected for color change.

Results:
Pass
(No Color Change)

Quantitative Halides (Cl, Br, FI) (Test #2.3.28.1)

Objective: The purpose of this test is to determine the total halide concentration of a flux.

Procedure: Flux is dissolved to a pre-determined concentration. Extracted solutions are then analyzed using an Ion Chromatograph with 3 to 5 level calibration. Total halide content is calculated and reported at Cl⁻ equivalent.

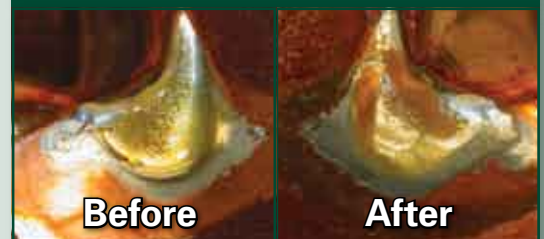
Results:
Total Halides
<0.5% Cl⁻ Equivalent

Qualitative Corrosion (Test #2.6.15)

Objective: The purpose of this test is to determine the corrosive properties of the flux residues under extreme environmental conditions.

Procedure: Solder paste is reflowed onto a sheet of copper and exposed to 40°C and 93% RH for 10 days. Coupon is then investigated for any signs of Cu corrosion.

Results and Image: Pass



Surface Insulation Resistance (Test #2.6.3.3)

Objective: The purpose of this test is to determine the Surface Insulation Resistance (SIR) of the flux residue after paste reflow.

Procedure: Paste is stenciled onto the test board and reflowed. The un-cleaned board is then sent to outside laboratory for testing.

Results: Pass

Surface Insulation Resistance (SIR), IPC-TM-650 Method 2.6.3.3 Results						
Coupon	Pattern	Initial	24 Hours	96 Hours	168 Hours	Final
1	A	1.95E+12	5.37E+07	2.34E+08	4.27E+08	1.07E+12
1	B	2.45E+12	5.37E+07	2.75E+08	4.79E+08	1.15E+12
1	C	1.48E+12	1.91E+08	2.24E+08	3.98E+08	1.00E+12
1	D	4.17E+11	5.50E+07	1.91E+08	3.63E+08	7.41E+11
2	A	1.91E+12	5.13E+07	3.02E+08	4.07E+08	1.15E+12
2	B	4.07E+11	6.17E+07	2.51E+08	4.37E+08	4.90E+11
2	C	1.38E+12	5.62E+07	2.19E+08	3.80E+08	7.76E+11
2	D	2.14E+12	6.03E+07	2.34E+08	4.07E+08	9.55E+11
3	A	3.02E+12	8.32E+08	2.19E+08	3.80E+08	7.94E+11
3	B	3.80E+12	6.03E+08	2.51E+08	4.37E+08	8.13E+11
3	C	4.07E+12	7.76E+07	3.02E+08	5.25E+08	1.00E+12
3	D	4.27E+12	6.61E+07	2.69E+08	4.68E+08	1.02E+12
Control 1	A	5.01E+12	5.37E+09	5.89E+09	3.98E+09	8.91E+11
Control 1	B	4.68E+12	5.50E+09	6.46E+09	3.55E+09	1.15E+12
Control 1	C	4.68E+12	5.25E+09	7.08E+09	3.89E+09	1.38E+12
Control 1	D	4.90E+12	5.50E+09	6.61E+09	3.55E+09	1.17E+12
Control 2	A	4.68E+12	1.95E+10	8.51E+09	8.13E+09	1.12E+12
Control 2	B	4.47E+12	1.62E+10	1.29E+10	7.76E+09	1.35E+12
Control 2	C	4.79E+12	8.13E+09	6.92E+09	5.75E+09	1.48E+12
Control 2	D	4.57E+12	1.17E+10	6.46E+09	4.79E+09	1.35E+12

Electrochemical Migration (Test #2.6.14.1)

Objective: The purpose of this test is to determine the Electrochemical Migration and SIR of the flux residue after paste reflow.

Procedure: Paste is stenciled onto the test board and reflowed. Un-cleaned board is then sent to outside laboratory for testing.

Results: Pass

Electrochemical Migration Resistance, IPC-TM-650 Method 2.6.14.1 Results				
Test Sample	Initial	96 Hour	500 Hour	Final
1	2.09E+12	1.82E+10	1.55E+10	4.79E+12
2	5.62E+12	6.03E+09	5.13E+09	4.37E+12
3	6.61E+12	7.76E+09	1.02E+10	5.62E+12
4	8.71E+12	2.09E+10	2.00E+10	6.03E+12
5	5.50E+12	2.88E+09	2.34E+09	3.98E+12
6	5.13E+12	2.04E+09	1.58E+09	3.24E+12
7	5.01E+12	2.04E+09	2.09E+09	3.80E+12
8	9.55E+12	3.31E+09	3.63E+09	4.68E+12
9	5.25E+12	1.41E+10	2.51E+10	5.13E+12
10	5.37E+12	4.47E+09	4.07E+09	4.37E+12
11	4.17E+12	6.03E+09	4.47E+09	5.13E+12
12	5.89E+12	1.66E+10	2.45E+10	5.75E+12
Geometric Mean (IR _{avg})	5.41E+12	6.37E+09	6.44E+09	4.67E+12
Control	Initial	96 Hour	500 Hour	Final
1	5.25E+12	1.26E+10	1.38E+10	4.27E+12
2	4.57E+12	1.00E+10	9.55E+09	3.89E+12
3	6.31E+12	1.15E+10	1.74E+10	4.68E+12
4	5.37E+12	1.95E+10	3.47E+10	4.90E+12
5	6.92E+12	3.98E+11	6.61E+11	4.79E+12
6	5.37E+12	8.13E+10	1.74E+11	4.37E+12
7	6.31E+12	1.00E+11	1.48E+11	5.13E+12
8	9.77E+12	3.89E+11	6.76E+11	6.17E+12
9	7.41E+11	5.62E+09	1.23E+10	3.80E+12
10	4.37E+12	1.12E+10	1.12E+10	3.16E+12
11	7.94E+12	1.32E+10	1.58E+10	3.89E+12
12	7.76E+11	2.00E+10	2.69E+10	5.13E+12
Geometric Mean (IR _{avg})	4.27E+12	3.03E+10	4.41E+10	4.45E+12

Note: add rows for coupons as needed.

IPC/J-STD-005 Test Results

Metal Content (Test #2.2.20)

Objective: The purpose of this test is to determine the weight percent of metal in the solder paste. The percentage should not deviate more than +/- 1% from the solder paste specification.

Procedure: A known weight of solder paste is reflowed in a glass beaker. A "button" of solder is formed from the coalescence of the solder. The "button" is cleaned and weighed. The ratio of "button" weight to original solder paste weight is the metal percent.

Sample Results	
Lot	Metal % (Type 3)
Sample 1	88.49
Sample 2	88.59
Sample 3	88.40
Sample 4	88.45
Sample 5	88.32

Viscosity (Test #2.4.34.2)

Objective: The purpose of this test is to determine the viscosity of a specific lot of solder paste. Viscosity testing is a fundamental test that ensures consistent performance from lot-to-lot.

Procedure: Approximately 500g of solder paste is stabilized at 25 +/- 1°C and the viscosity is measured using a Malcom spiral pump viscometer at 5rpm's. The results are measured and compared to the nominal value. Solder paste lots with values outside the expected variation (USL and LSL) need to be investigated for possible performance related issues.

Sample Results									
Lot Number	10 rpm (3 min)	3 rpm (6 min)	4 rpm (3 min)	5 rpm (3 min)	10 rpm (3 min)	20 rpm (1 min)	30 rpm (1 min)	10 rpm (1 min)	SSF
Sample 1	2205	5693	4525	3842	2273	1489	1147	2212	-0.6935
Sample 2	2190	5829	4562	3850	2280	1436	1102	2132	-0.7199
Sample 3	2058	4935	4010	3421	2062	1379	1150	2105	-0.6424
Sample 4	1902	4797	3882	3244	1908	1281	998	1890	-0.6833
Sample 5	1867	4753	3820	3228	1916	1229	968	1841	-0.6949

Solder Ball (Test #2.4.43)

Objective: The purpose of this test is to validate soldering performance of a specific lot of solder paste. Solder ball testing is a fundamental test that ensures consistent performance for lot-to-lot.

Procedure: Three small deposits of solder paste are printed onto a ceramic coupon and reflowed at a temperature of approximately 240°C (for Sn/Ag/Cu alloys). The coupon is then inspected to ensure complete coalescence of the solder paste, and that there are no extraneous solder balls in the flux pool. Results are compared to images in the J-STD-005 to determine whether it passes or fails.

Typical Result and Image: Pass, Preferred



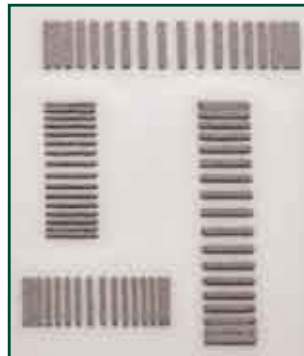
Slump (Test #2.4.35)

Objective: The purpose of this test is to determine the potential for slumping with a given solder paste.

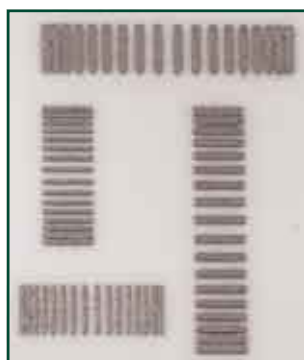
Procedure: For cold slump, solder paste is printed using an IPC-A-20 stencil on an alumina substrate and examined for maximum spacing bridged. Samples are stored at 47% relative humidity at room temperature (approx. 25 +/- 5°C) for 20 minutes. Samples are then re-examined for maximum spacing bridged. For hot slump, samples are again printed with an IPC-A-20 stencil on an alumina substrate and examined for maximum spacing bridged. Samples are then heated to 180°C for 15 minutes and allowed to cool. Samples are re-examined immediately, and again after 2-hours and 4-hours, for maximum spacing bridged.

Result: Pass Solder Paste - Slump Test (IPC-TM-650 2.4.35)

180°C



Room Temperature



Wetting (Test #2.4.45)

Objective: The purpose of this test is to ensure that the solder paste has sufficient capability to wet to a copper substrate.

Procedure: Solder paste is printed onto a clean copper coupon and reflowed using the manufacturers recommended reflow profile. The coupon is then inspected to ensure uniform wetting and no evidence of de-wetting or non-wetting.

Results and Image: Pass

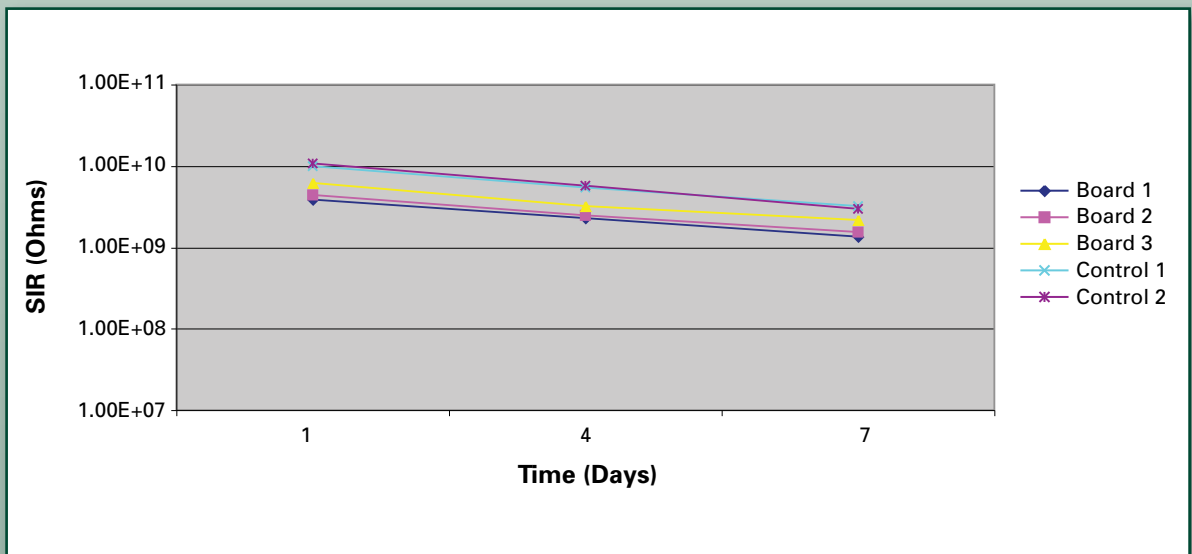


Compatibility

Indium8.9

SIR Test Data with WF-9942, CW-801, and TACFlux®20B

Results: Pass				
Surface Insulation Resistance (SIR), IPC-TM-650 Method 2.6.3.3 Results				
Coupon	Pattern	24 Hours	96 Hours	168 Hours
1	A	4.79E+09	2.82E+09	1.58E+09
1	B	3.55E+09	2.09E+09	1.29E+09
1	C	3.39E+09	2.09E+09	1.15E+09
1	D	3.80E+09	2.24E+09	1.35E+09
2	A	4.27E+09	2.82E+09	1.62E+09
2	B	4.27E+09	2.29E+09	1.48E+09
2	C	4.47E+09	2.40E+09	1.48E+09
2	D	4.47E+09	2.45E+09	1.58E+09
3	A	7.76E+09	4.27E+09	2.88E+09
3	B	6.17E+09	3.24E+09	2.19E+09
3	C	5.13E+09	2.45E+09	1.55E+09
3	D	6.03E+09	2.88E+09	2.04E+09
Control 1	A	1.00E+10	5.37E+09	3.16E+09
Control 1	B	9.12E+09	4.68E+09	2.88E+09
Control 1	C	1.07E+10	5.89E+09	3.47E+09
Control 1	D	1.02E+10	5.62E+09	3.24E+09
Control 2	A	1.20E+10	6.03E+09	3.16E+09
Control 2	B	1.02E+10	5.25E+09	2.88E+09
Control 2	C	1.12E+10	6.03E+09	3.02E+09
Control 2	D	1.00E+10	5.50E+09	2.88E+09



IPC/J-STD-006 Test Results

Example of Certificate of Analysis and Conformance for Solder Powder Products

PRODUCT CERTIFICATION

Product: 96.5Sn 3.0Ag .5Cu / -325+500

Alloy Integrity			Reported by: LAZ	
Major Elements:	Sn	96.390 %	Test Method(s):	AC
	Ag	3.068 %		
	Cu	0.507 %		


RoHS Compliance:			Impurities	
	<i>Actual</i>	<i>RoHS Max</i>	-----	
	Pb	0.0132%	0.0021% Bi	
	Cd	Not Detected	0.0026% Fe	
	Total Cr	Not Detected	0.003% In	
	Hg	Not Detected	0.0132% Pb	
			0.0118% Sb	
Indium certifies that this product meets RoHS requirements if Pb or Cd is not a part of the alloy constituency. Any product that is <99.9% pure is not certified to be RoHS compliant. Review ROHS directive for any applicable exemptions. Indium does not use any flame retardant in its product.			Total: 0.0327% (327 PPM) >99.9% Pure	

Powder Size Distribution:			Oxide: 0.069 %	
+270	-	0%	Reported by:	KMB
-270/+325	-	1.1%	Test Method(s):	BD
-325/+400	-	36.1%	Visual Inspection:	<input checked="" type="checkbox"/> Acceptable
-400/+450	-	31.5%	Reported by:	KMB
-450/+500	-	30.5%	Test Method(s):	MS @ 100x
-500/+635	-	0.6%		
-635	-	0%		
Reported by:	PR			
Test Method(s):	SA			

Comments:

CONFORMANCE STATEMENT

Indium Corporation of America certifies that all the material used in the manufacture of this order has been made in accordance with its standard procedures and practices. Test reports to substantiate the same are retained in Indium Corporation's files and are available for your examination during the agreed upon time.


Director, Corporate Quality

APPROVING OFFICER



Nicole A. Palma
Quality Technician

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- Feasibility studies for new technologies and materials
- Reflow profile optimization



Indium's Process Simulation Lab Capabilities:

- | | |
|--|---|
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| • Precision syringe dispensing | • Temperature-humidity-bias testing (SIR & ECM) |
| • Fully automated 3D solder paste inspection | • Mechanical strength testing |
| • Component placement | • TG/DTA & DSC analysis |
| • Forced air convection and infrared reflow | • Wetting balance testing |
| • Wave soldering | • Thermal cycling |
| • X-ray analysis | • And more... |



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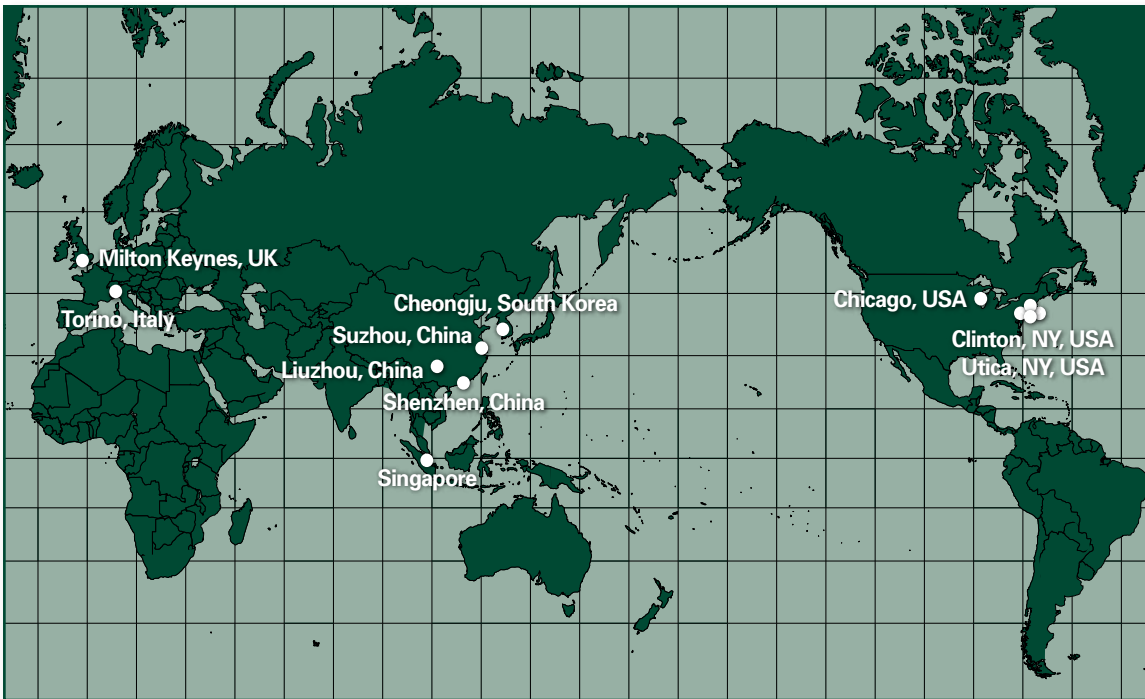
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